UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,523	04/25/2006	Masahiro Nakayama	039.0071	2166

29453 7590 04/13/2011

Judge Patent Associates
Vert Nakanoshima Kita, Suite 503
6-3 Nishitemma 4-Chome, Kita-ku
Osaka-Shi, 530-0047
JAPAN

EXAMINER	
LEE, JAE	

ART UNIT	PAPER NUMBER
2895	

MAIL DATE	DELIVERY MODE
04/13/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,523	NAKAYAMA ET AL.	
	Examiner	Art Unit	
	JAE LEE	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,11 and 12* is/are pending in the application.

4a) Of the above claim(s) *3 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,11,12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Applicant Arguments, filed 02/04/2011, with respect to the rejection(s) of claim(s) 1 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Ito (Pub No. US 2003/0203657 A1, hereinafter Ito).

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoki et al. (USP# 6,468,347 B1, hereinafter Motoki) and further in view of Ito.

With regards to claim 1, Motoki teaches a gallium-nitride semiconductor substrate having a mirrorlike, planar surface directly onto which a light-emitting-device-forming film has been epitaxially grown (see Fig. 21a-Fig. 21e).

Motoki, however, does not teach the gallium-nitride substrate therein contaminated at the interface between the mirrorlike, planar surface and the device-forming film grown thereon by one or more elements selected from Si, Cr, Mn, Fe, Ni, Cu, Zn and Al at a density level of from 15×10^{10} to 10×10^{11} atoms/cm^2.

In the same field of endeavor, Ito teaches a cleaning method wherein nickel impurities are removed form the surface of an SOI to a level lower than the claimed range (see ¶40, $1x10^9$ atoms/cm^2 obtained on surface of SOI), wherein the SOI could be a GaN layer (see ¶114). One of ordinary skill would strive to achieve the lowest level of metal contamination possible in order to prevent short circuiting effects or other layer mishaps. Furthermore, if a lower level of metal contamination that the one claimed can be achieved according to Ito, then one of ordinary skill may certainly achieve the claimed range.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to utilize the method of Ito to produce contaminant levels claimed since Ito clearly demonstrated that lower contaminant levels can be achievable. One of ordinary skill would strive to achieve the lowest level of metal contamination possible in order to prevent short circuiting effects or other layer mishaps. Furthermore, if a lower level of metal contamination that the one claimed can be achieved according to Ito, then one of ordinary skill may certainly achieve the claimed range.

With regards to claim 2, Motoki teaches a gallium-nitride semiconductor substrate having a mirrorlike, planar surface directly onto which a light-emitting-device-forming film has been epitaxially grown (see Fig. 21a-Fig. 21e).

Motoki, however, does not teach the gallium-nitride substrate therein contaminated at the interface between the mirrorlike, planar surface and the device-

forming film grown thereon by one or more elements selected from Si, Cr, Mn, Fe, Ni, Cu, Zn and Al at a density level of from 15 x 10^{10} to 5 x 10^{11} atoms/cm^2.

In the same field of endeavor, Ito teaches a cleaning method wherein nickel impurities are removed form the surface of an SOI to a level lower than the claimed range (see ¶40, 1x10^9 atoms/cm^2 obtained on surface of SOI), wherein the SOI could be a GaN layer (see ¶114). One of ordinary skill would strive to achieve the lowest level of metal contamination possible in order to prevent short circuiting effects or other layer mishaps. Furthermore, if a lower level of metal contamination that the one claimed can be achieved according to Ito, then one of ordinary skill may certainly achieve the claimed range.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to utilize the method of Ito to produce contaminant levels claimed since Ito clearly demonstrated that lower contaminant levels can be achievable. One of ordinary skill would strive to achieve the lowest level of metal contamination possible in order to prevent short circuiting effects or other layer mishaps. Furthermore, if a lower level of metal contamination that the one claimed can be achieved according to Ito, then one of ordinary skill may certainly achieve the claimed range.

With regards to claims 11 and 12, Motoki teaches a gallium-nitride semiconductor substrate as set forth in claims 1 and 2, wherein the substrate surface on which the device-forming epitaxial film has been grown is a complex of faces in which

Ga is exposed, and faces in which N is exposed (the gallium nitride substrate taught by Motoki will have exposed faces of gallium atoms and nitrogen atoms when the structure of gallium nitride is viewed at the atomic level).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAE LEE whose telephone number is (571)270-1224. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae Lee/
Examiner, Art Unit 2895

JML